REMARKS

Claims 1-19 are currently pending in the application. By this amendment, claim 12 is amended to correct a minor typographical error pointed out by the Examiner. Applicants submit that no new matter has been entered. Support for the amendment can be found in paragraph [0035] and Figure 2. Reconsideration of the rejected claims in view of the above amendment and the following remarks is respectfully requested.

Entry of Amendment Proper

Applicants submit that the entry of the above amendment is proper. Applicants submit that the amendments do not add any new issues which need further search and/or consideration. The amendments made herein are to correct minor formalities only. Applicants further submit that the entry of the amendments is proper since such amendments place the application in condition for allowance or, alternatively, place the application in better form for appeal.

Objection to the Drawings

The drawings were objected to for failing to comply with 37 C.F.R. 1.84(p)(4) and for failing to comply with 37 C.F.R. 1.84(g). Applicants have submitted herewith amended drawings, incorporating descriptive labels as suggested by Examiner. Additionally, the margins of Figure 2 have been increased. Applicants submit that no new matter has been entered. For example, support for the descriptive labels can be found at least at paragraphs [0016] – [0025].

Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

35 U.S.C. § 102 Rejection

Claims 1 – 11 and 19 were rejected under 35 U.S.C. § 102(e) for being anticipated by U.S. Patent 6,092,225 issued to Gruodis et al. (hereinafter Gruodis). Claims 12 – 18 were rejected under 35 U.S.C. § 102(e) for being anticipated by U.S. Patent 5,872,797 issued to Theodoseau (hereinafter Theodoseau). These rejections are respectfully traversed.

To anticipate a claim, each and every element set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. MPEP § 2131. Applicants submit that neither Gruodis nor Theodoseau disclose each and every feature of the claimed invention.

Rejection of Independent Claims 1 and 19 over Gruodis

The present invention generally relates to a method and system for testing an electronic circuit. More specifically, claim 1 recites, in pertinent part:

> defining a first initial vector;
> defining at least one segment within the first initial vector;
> offsetting the first initial vector a predetermined amount within the at least one segment;
> defining a counter loop comprising loops of the first initial vector within the at least one segment to produce a first set of vectors in accordance with the counter loop;
> defining a progressively changing variation of the first initial vector for each loop of the counter loop so at least one vector of the first set of vectors varies from the first initial vector;
> and coupling the at least one segment having the first set of vectors including the varied at least one vector to produce a final pattern for a circuit under test.

Claim 19 recites, in pertinent part:

> define a first initial vector;
> define at least one segment within the first initial vector;
> offset the first initial vector a predetermined amount within the at least one segment;

define a counter loop comprising loops of the first initial vector within the at least one segment to produce a first set of vectors in accordance with the counter loop;

define a progressively changing variation of the first initial vector for each loop of the counter loop so at least one vector of the first set of vectors varies from the first initial vector; and

coupling the at least one segment having the first set of vectors including the varied at least one vector to produce a final pattern for a circuit under test.

The Examiner asserts that Gruodis discloses these features in column 3, lines 49 – 62, column 4, line 10 to column 6, line 51, column 5, lines 22 – 32, and column 11, lines 30 – 45. Applicants respectfully disagree.

Gruodis discloses an integrated circuit tester that organizes an IC test into a succession of test cycles, each test cycle being divided into four segments. More specifically, Gruodis discloses at column 5, lines 22 – 33 that:

> Cache memory system 28 responds to the CACHE_OP opcode by supplying those sixteen vectors VAA – VAH, VBA – VBH to a "vector alignment" circuit 30.
>
> Instruction processor 26 also generates alignment control signals ALIGN_CONT for controlling vector alignment circuit 30. Vector alignment circuit responds to the ALIGN_CONT by selecting four vectors from the multiple vectors read out of the cache memory system 28 and providing them as output at the start of the next test cycle for controlling test activities of the test channel during the test cycle.

Additionally, Gruodis discloses at column 11, lines 31 – 45:

> FIG 5 illustrates vector alignment circuit 30 of FIG. 1 in more detailed block diagram form. Referring to FIG. 5, vector alignment circuit 30 includes a register 4 clocked by the PCLK signal for delaying the sixteen output vectors VAA – VAH, VBA – VBH of cache memory system 28 of FIG. 1 by one test cycle and applying then [sic] as inputs to a routing switch 62. Routing switch 62 also directly receives the sixteen output vectors VAA – VAH, VBA – VBH of cache memory system 28 of FIG. 1. Routing switch 62, suitably a cross point switch or a tree of multiplexers, produces the four vectors VA – VD supplied to formatter 16 of FIG. 1 by selecting them from among its 32 input vectors in response

to the alignment control data ALIGN_CONT from instruction processor 26 of FIG. 1.

Specifically, the Examiner designated the first initial vector as the set of four vectors (VA – VD) at the start of each cycle, and the Examiner asserted that the vector alignment circuit 30 of Gruodis discloses offsetting the first initial vector a predetermined amount within the at least one segment, as recited in claim 1. More specifically, the Examiner stated in his response to arguments that " . . . Gruodis' vector alignment circuit 30 offsets or delays the vectors within the segments (Col. 11, ll. 30 – 45, delays the sixteen output vectors)." Applicants submit, however, that the vector alignment circuit does not offset the first initial vector a predetermined amount within the at least one segment.

Applicants acknowledge that Gruodis discloses the vector alignment circuit including a register for delaying the sixteen vectors of the cache memory system by one test cycle and applying them as inputs to the routing switch. However, Applicants submit that the sixteen vectors VAA – VAH and VBA – VBH are not the first initial vector (designated as VA – VD). Moreover, while the sixteen vectors VAA – VAH and VBA – VBH are delayed, this occurs prior to the creation of the initial vector (designated as VA – VD). Rather, Applicants submit that the vectors VA – VD, designated by the Examiner as the initial vector, are selected from among the sixteen vectors VAA – VAH and VBA – VBH, subsequent to the sixteen output vectors being delayed.

As such, Applicants submit that Gruodis does not disclose offsetting the first initial vector a predetermined amount within the one segment. Therefore, Gruodis does not contain each and every element of the claim, and does not anticipate the claimed invention.

Rejection of Dependent Claims 2 – 11 over Gruodis

Applicants respectfully submit that claims 2 – 11 depend from a distinguishable independent claim, and are allowable based upon the allowability of the independent claim.

Additionally, Applicants submit that Gruodis does not disclose defining a second vector; allocating a second segment configured to contain the second vector; and offsetting the second vector a predetermined amount within the second segment, as recited in claim 10. As discussed with regards to claim 1, Applicants submit that the "delaying" disclosed by Gruodis is not a delaying of the second vector, but rather a delaying of the 16 vectors VAA – VAH and VBA – VBH from which the vectors VA – VD are produced. Therefore, Gruodis does not contain each and every element of the claim, and does not anticipate the claimed invention.

Accordingly, Applicants respectfully request that the rejection over claims 1 – 11 and 19 be withdrawn.

Rejection of Independent Claim 12 over Theodoseau

The present invention generally relates to a method and system for testing an electronic circuit. More specifically, claim 12 recites, in pertinent part:

> selecting a macro definition file defining at least one vector;
> forming a control bit definition file configured to be added to the at least one vector;
> creating a pattern definition file configured to selectively alter a portion of the at least one vector;
> creating a global definition file configured to alter the entire vector; and
> combining the macro, control bit, pattern, and global definition files to form a final vector to produce a final pattern.

The Examiner asserts that Theodoseau discloses these features in column 6, line 36 to column 9, line 50. Applicants respectfully disagree.

Theodoseau discloses a user-specified nested sequence of counters, logical combination of the counter outputs and generation of corresponding vectors for application to exercise integrated circuit devices. More specifically, Theodoseau discloses a counter control 402 that controls the organization of the vectors, or sequences of vectors, selected by the pattern control selector 420, and the order of their selection with the read and write macros in accordance with timing groups provided by element 425. In other words, the counter control 402, in conjunction with the timing groups 425, causes the pattern control selector 420 to function as a scheduler for the vectors and macros and counting therein into a complete test or burn-in sequence.

The Examiner asserts that Theodoseau discloses combining the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern. Applicants submit, however, that, assuming *arguendo* a macro definition file defining at least one vector is taught by Theodoseau's read macro or write macro, and the creation of a global definition file configured to alter the entire vector is taught by Theodoseau's refresh macro, which Applicants do not concede, Theodoseau does not disclose combing the macro, control bit, pattern formats, and global definition files to form a final vector to produce a final pattern. Instead, Theodoseau specifically discloses that a vector is developed "in accordance with the counter control 402 and one of read macro 406, write macro 404 or refresh macro 408 as may be selected by pattern control selector . . . ." (column 7, lines 10+).

Thus, Applicants submit that the Examiner's interpretation of Theodoseau runs counter to the explicit disclosure of Theodoseau. Specifically, the Examiner asserts Theodoseau's use of both a read or write macro, and a refresh macro. In contrast, Theodoseau discloses the use of a read macro, write macro or refresh macro in developing a vector. Therefore, Theodoseau does not contain each and every element of the claim, and does not anticipate the claim.

Rejection of Dependent Claims 13 – 18 over Theodoseau

Applicants respectfully submit that claims 13 – 18 depend from a distinguishable independent claim, and are allowable based upon the allowability of the independent claim.

Accordingly, Applicants respectfully request that the rejection over claims 12 – 18 be withdrawn.

CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,
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